

ABSTRACT OF THE DISCLOSURE

A memory device is constructed by connecting a plurality of flat high-speed memory modules each including a connector on one side of which input side and output side terminals for dealing with a high-speed signal of plural-bit width whose impedance is controlled and which is transmitted from a memory controller to a terminal resistor are arranged. The memory device in which memory modules can be cascade-connected and which can maintain the impedance of a memory bus signal in a constant value by use of an inexpensive multi-layered circuit board structure is provided. A socket mounting structure of the memory device and a mounting method of the memory device is provided.